Consolidated Statement of Result for M.Tech (ECE) 2nd Semester, July 2020

8/5/2020

Sr. No.	Student's Name	Registration Number	Research Ethics(ROC102)	Device Modeling & Circuit Simulation (MVD102)	Digital System Design with FPGA (MVD104)	Deep Submicron CMOS Ics (MVD106)	Digital VLSI Design (MVD110)	Digital System Design using Verilog (MVD122)	SGPA
			Grade	Grade	Grade	Grade	Grade	Grade	
1	SHAMBHAVI TIWARI	00102122019	C+	B+	C+	B	B+	A	7.39
2	SABITA KUMARI	00202122019	C	B+	B+	C+	B	A	7.26
3	NAVDHA VERMA	00302122019	C+	B+	C+	B	A	A	7.57
4	RAMSHA SUHAIL	00402122019	B+	B+	B+	B+	B+	A	8.17
5	ANUSHKA DIXIT	00502122019	B	B+	B+	C+	A	A	7.87
6	PALAK HANDA	00602122019	B+	B+	B	B	A+	A	8.17
7	KANIKA SHARMA	00702122019	C+	B+	B	B	A+	A	7.91
8	ANUKRITI	00802122019	C	B+	C+	C+	A	A	7.26
9	SAMRIDHI SETHI	00902122019	B	B+	A	B+	B+	A	8.22
10	SHILPA C. LALU	01002122019	B	B+	B	B	A+	A	8.04
11	NEELU TIWARI	01102122019	B	B+	B	B+	A	A	8.04

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